A DC HYBRID CIRCUIT BREAKER BASED ON TWO-STAGE COMMUTATION

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ABSTRACT

A new topology of DC hybrid circuit breaker based on two-stage commutation has been proposed in this paper. In normal current breaking, the current is commutated by utilizing the arc voltage across high-speed switch (HSS). In fault current breaking, the current is cummutated in two stages, which not only achieves the arcless open of HSS, but also lowers the over-voltage rate of rise. The influence of the arc voltage on the commutation time and arc energy in normal current breaking is investigated experimentally. Then, the simulation model of the fault current breaking under different current rates of rise in medium voltage DC (MVDC) system is established on MATLABSIMULINK platform. Finally, the breaking over-voltages for the single-stage and two-stage commutation topologies in fault current breaking are compared. The simulation results show that the topology with two-stage commutation can improve the breaking reliability greatly.

1. INTRODUCTION

With the rapid development of transmission and distribution network in the modern power system, DC grids are paid more and more attention for its significant advantages of low loss and no reactive power. However, the fact of no natural zero crossing and high rising rate of fault current in DC power system leads to that the current rises rapidly to dozens or even hundreds of kA in extremely short time [1]. The handling of fault current has become a critical issue to improve the power quality in DC system, especially in the medium-voltage and high-voltage grids [2]. Traditional AC high-power mechanical circuit breakers, which all depend on current zero crossing to realize the breaking, can not satisfy the breaking requirements in DC system [3]. Recently, DC hybrid circuit breaker based on high-speed switch (HSS) and parallel connected capacitor has gained interest [4,5,6]. With fast responding speed and short breaking time of DC hybrid circuit breaker, the fault current can be broken long before it reaches the expected maximum level. However, as the parallel connected capacitor needs to absorb the energy stored in system inductance within very short time [7], the over-voltage rate of rise is extremely high in the breaking process, which may cause breakdown between the contacts of HSS. In view of this, a new topology of DC hybrid circuit breaker based on two-stage commutation is proposed. In normal current breaking, the circuit breaker utilizes arc voltage across the contacts of HSS to commutate the current. In fault current breaking, the parallel connected capacitor is used to commutate the fault current, which not only achieves the arcless open of HSS, but also lowers the over-voltage rate of rise in the breaking significantly. In addition, the polarity of capacitor voltage keeps consistent with that before the breaking, avoiding the recharging before next operation.

Fig. 1 shows the topology of DC hybrid circuit breaker based on two-stage commutation. VT_1 and VT_2 are both fast thyrisors. VD_0 and VD_1 are diodes. IGCT is the integrated gate controlled thyristor. C is commutation capacitor.

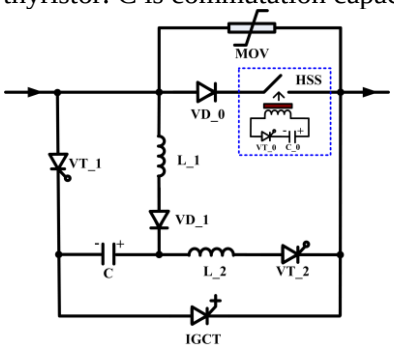

Fig. 1 The topology of DC hybrid circuit breaker based on two-stage commutation

2. ANALYSIS OF THE NORMAL CURRENT BREAKING PROCESS

In the normal current breaking, HSS is controlled to open at first. Then, VT_1 and IGCT are turned on. The current is commutated from VD_0-HSS to VT_1-IGCT by utilizing the arc voltage across HSS. Finally, the current is commutated to MOV after IGCT is turned off and the breaking is completed when the current in MOV drops to zero.

When the current is commutated from HSS to IGCT, the arc is generated in HSS. It will significantly affect the dielectric breakdown strength between the contacts. Hence, the commutation time and arc energy under different arc voltages should be determined in normal current breaking process. Fig. 2 shows the testing circuit diagram of the current commutation in normal current breaking. HSS is air high-speed switch [8]. R is resistance of 0.2Ω.

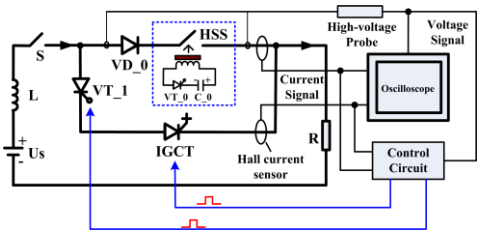

Fig. 2 The testing circuit diagram of the current commutation in the normal current breaking

Fig. 3 shows variations of the arc voltage across HSS and contact opening distance versus the breaking time in the case of 5 kA. As the arc voltage is far less than the system voltage, it can be considered that the current in HSS is identical. Therefore, the arc voltage between contacts varies mainly with the contact opening distance.

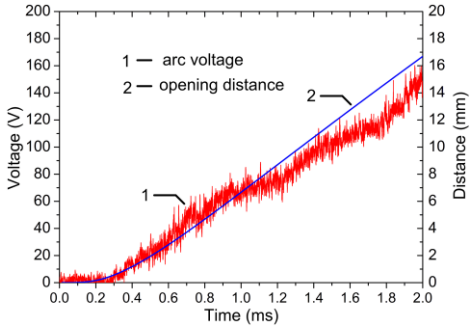

Fig. 3 The variations of the arc voltage across HSS and contact opening distance versus the breaking time in the case of 5 kA

Table 1 gives the commutation time and arc energy for different arc voltages. As can be seen, with arc voltage increasing, the current commutation time becomes shorter. Meanwhile, the arc energy increases obviously, which implies that it will take longer time for the dielectric recovery of the contacts. Therefore, VT_1 and IGCT should be turned on at the moment when the arc is ignited.

Table 1 The commutation time and arc energy for different arc voltages in normal current breaking

Arc voltage (V)	60	80	100	120
Commutation time (us)	165	130	105	85
Arc energy (J)	108	172	276	465

3. ANALYSIS OF THE FAULT CURRENT BREAKING PROCESS

Fig. 4 shows the operation principle of the first commutation process during the fault current breaking. In normal current flowing, HSS and VD_0 carry the rated current (Fig. 4(a)). When the fault occurs, i rises rapidly. Then HSS is controlled to operate at first. Due to the mechanical delay time of HSS, the contacts of HSS are still in the closed state. Afterwards, VT_1 and VT_2 are turned on and i_1 is commutated into VT_1-C-L_2-VT_2 (Fig. 4(b)). After i_1 is fully commutated, the contacts of HSS are opened without arc (Fig. 4(c)). Along with the capacitor charged by i_2, the capacitor voltage is reversed, So the current is commutated from VT_1-C to L_1-VD_1 and the capacitor continues to be charged (Fig. 4(d)). Finally, the current is completely commutated and VT_1 is turned off (Fig. 4(e)).

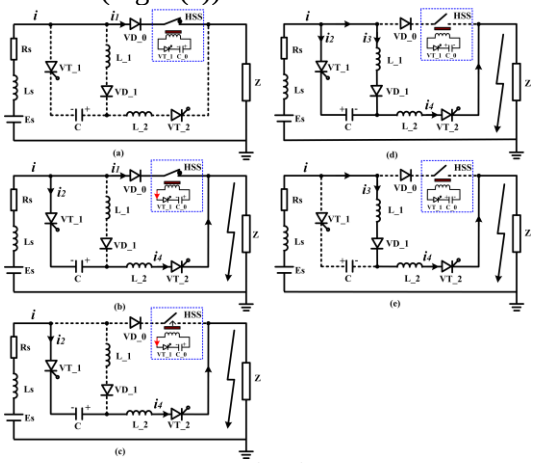

Fig. 4 The operation principle of the first commutation process

Fig. 5 shows the operation principle of the second commutation process during the fault current breaking. When IGCT is turned on, i_4 starts to be commutated to C- IGCT (Fig. 5(a)). Then the current all flows through L_1-VD_1-C-IGCT, leading to that i_4 becomes zero (Fig. 5(b)).

With the capacitor charged by i_5, the polarity of capacitor voltage is changed again (Fig. 5(c)). Finally, when the voltage across L_1-VD_1-C-IGCT reaches the turn-on voltage of MOV, i_5 is commutated to MOV (Fig. 5(d)). As the voltage across MOV opposes the system voltage (Es), i_6 drops fast. The whole breaking is accomplished when i_6 decreases to zero.

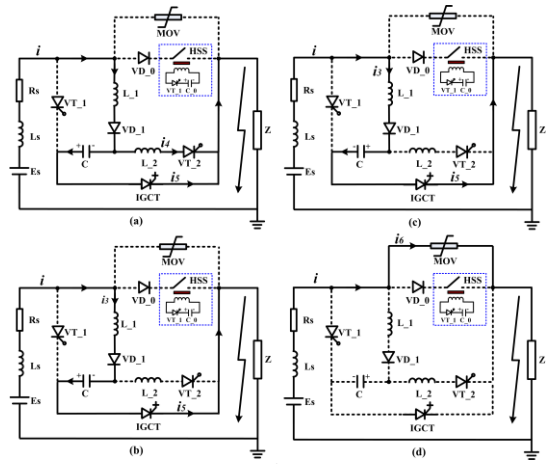

Fig. 5 The operation principle of the second commutation process

As seen from the above process, the topology based on the two-stage commutation can not only realize the arcless open of HSS, but also keep the polarity of capacitor voltage consistent with that before the breaking.

The simulation model of fault current breaking in 10kV MVDC system is constructed on MATLABSIMULINK platform. The simulation parameters are given in Table 2. The mechanical delay time of HSS is 270us and the turn-on voltage of MOV is 15kV. Ls is separately taken 850, 630 and 410uH with their corresponding current rates of rise (*di/dt*) of 10,15 and 20A/us.

Table 2 Parameters of simulation model

System voltage	Es	10kV
System inductance	Ls	410, 630 and 850uH
System resistance	Z	3Ω
Circuit resistance	Rs	100mΩ
Commutation capacitance	C	0.5mF
Capacitor voltage	U_C	5kV
Inductance 1	L_1	60uH
Inductance 2	L_2	30uH
Current trigger value	Is	5kA

Fig. 6 shows the current and voltage waveforms for different *di/dt* in the fault current breaking. It can be seen that the topology can realize the successful breaking under different fault conditions. As *di/dt* increases, the breaking time decreases, with 3.6, 3.1 and 2.7 ms respectively, which is beneficial for limiting the maximum value of fault current. When the current is completely commutated from VT_1-C to L_1-VD_1, the voltage across L_1 drops fast, leading to that the voltage across hybrid circuit breaker (u_{HCB}) reduces rapidly. Since the capacitor is reversely pre-charged after the first commutation, the voltage across L_2 and VT_2 is turned into the capacitor voltage when IGCT is turned on, which can further lower u_{HCB}.

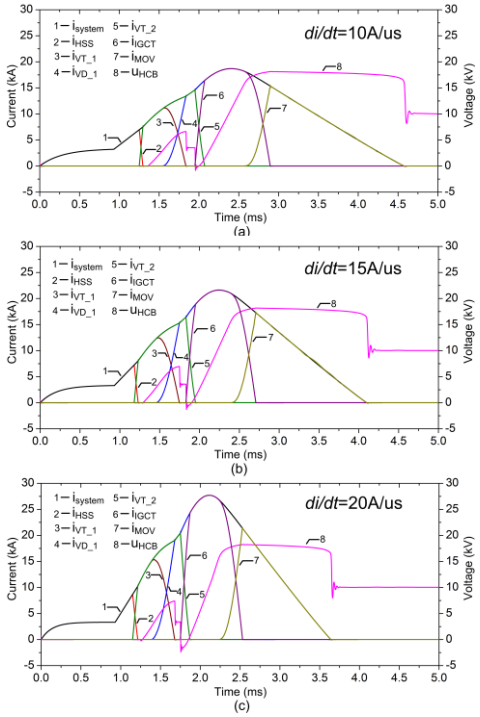

Fig. 6 The current and voltage waveforms for different di/dt in the fault current breaking

Fig. 7 describes the testing circuit diagram of single-stage commutation topology, in which the parameters are the same as those in Table 1. The current through HSS is commutated via the parallel capacitor, thereby realizing the arcless open of HSS.

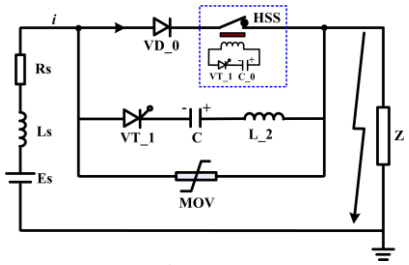

Fig. 7 The testing circuit of single-stage commutation topology

The simulation result of the single-stage commutation topology in the fault current breaking is given in Fig. 8. Compared with the two-stage commutation, the single-stage commutation topology has shorter breaking time and smaller peak value of fault current owing to rapid rising of the capacitor voltage.

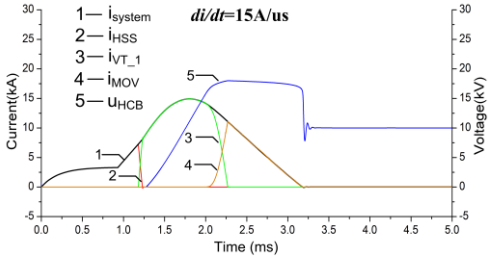

Fig. 8 The simulation result of single-stage commutation topology in the fault current breaking

Fig. 9 shows the over-voltages of single-stage and two-stage commutation topologies during the fault current breaking with *di/dt*=15A/us. Wherein, the withstand voltage between the contacts is tested experimentally. At t0=1.05 ms, HSS is controlled to operate and then the contacts are opened at t1=1.3 ms with the withstand voltage of U1. It can be seen that u_{HCB} of single-stage commutation is higher than the withstand voltage from t2=1.7 ms to t3=2.3 ms, which may cause breakdown between the contacts. However, u_{HCB} of two-stage commutation becomes fairly lower after 1.6 ms, which implies a successful breaking.

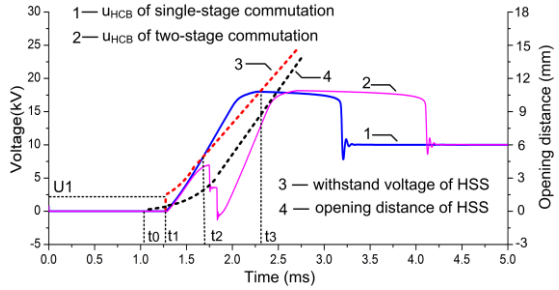

Fig. 9 The over-voltages of single-stage and two-stage commutation topologies with di/dt=15A/us

4. CONCLUSION

A new topology of DC hybrid circuit breaker based on the two-stage commutation is proposed. The influence of arc voltage across HSS on the commutation time and arc energy in normal current breaking is analyzed experimentally. The higher the arc voltage, the longer recovery time HSS needs. The simulation model of the fault current breaking under different conditions in MVDC system is developed. Meanwhile, the breaking over-voltages for the single-stage and two-stage commutation topologies are compared. The simulation results show that the topology with two-stage commutation can not only achieve the arcless open of HSS, but also reduce the over-voltage rate of rise notably. Hence, the breaking reliability can be improved greatly. Moreover, the polarity of capacitor voltage is consistent with that before the breaking, avoiding the recharging after operation.

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